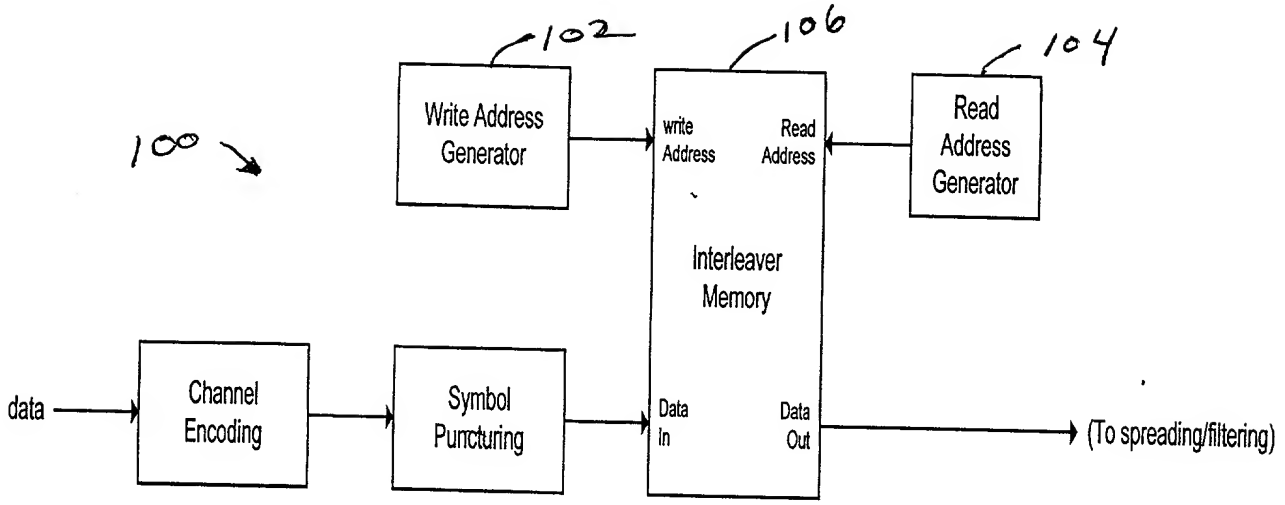
FIG. 1



Prior Art

FIG. 2A

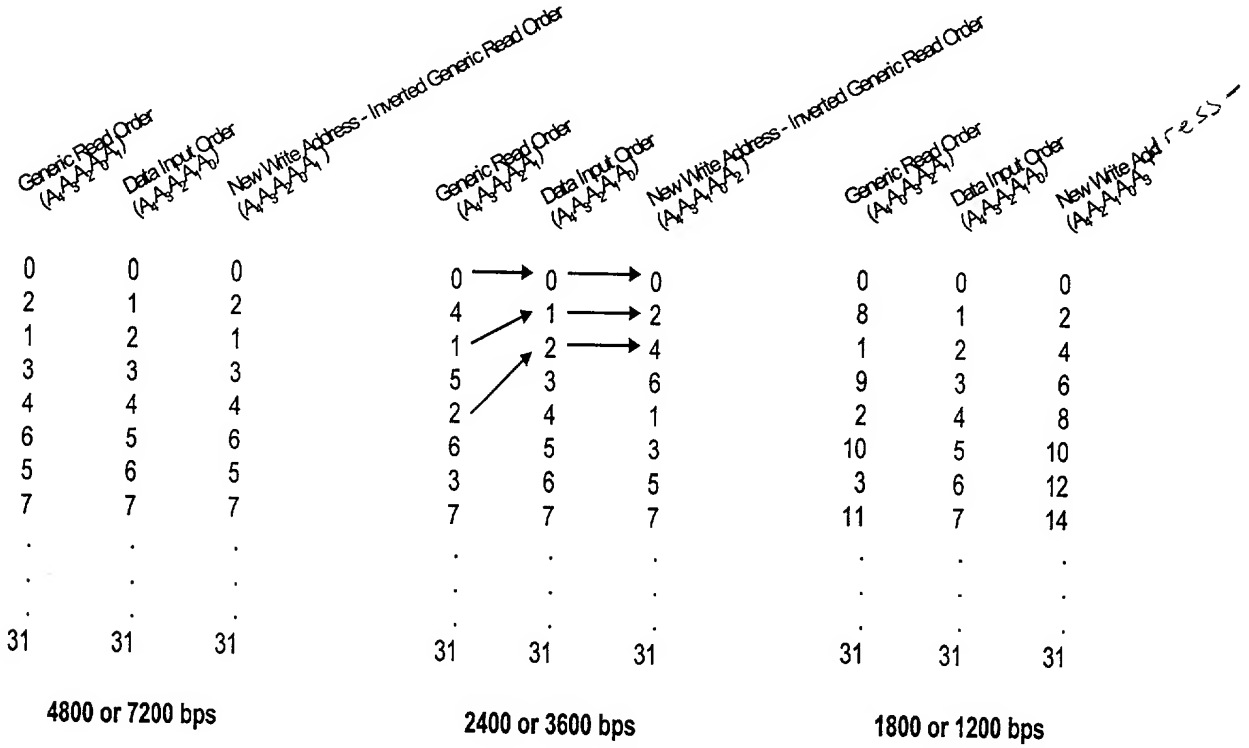


FIG. 2B

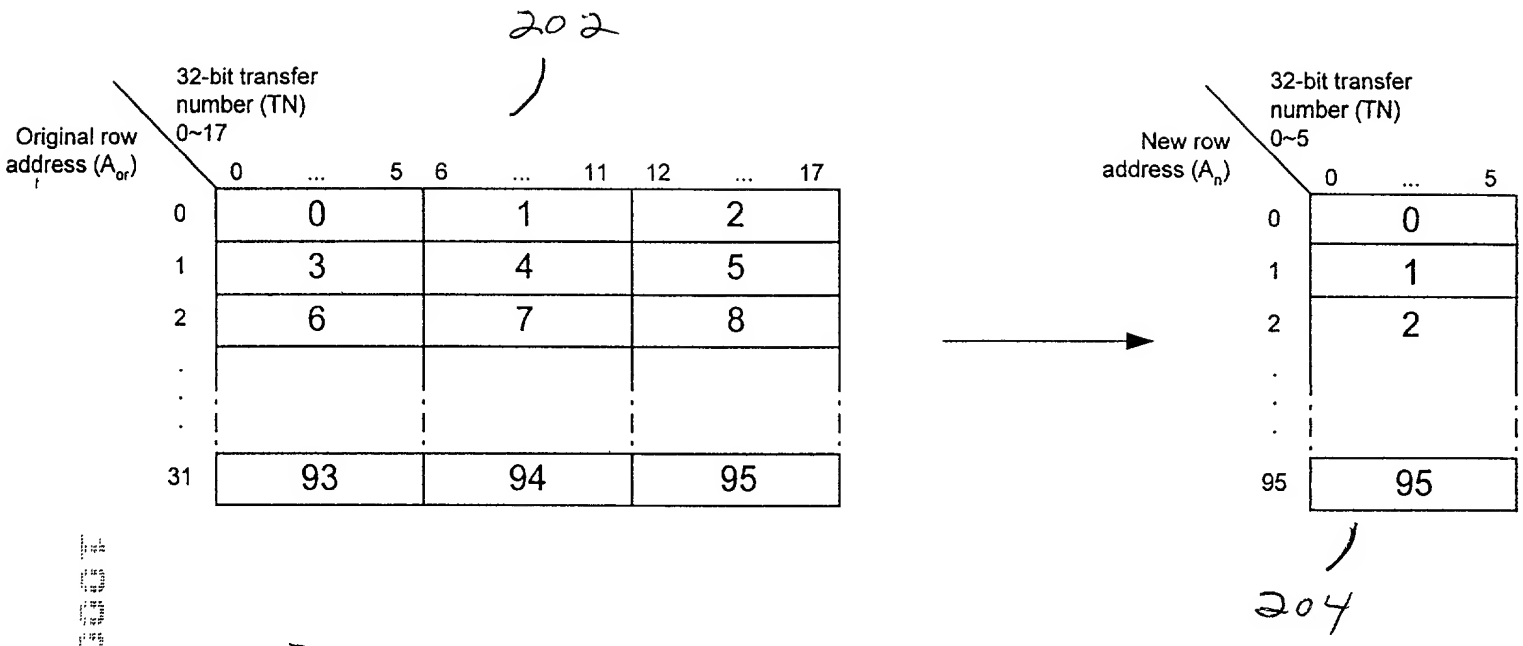

202
32-bit transfer number (TN) 0~17
Original row address (A_{or})
0 ... 5 6 ... 11 12 ... 17
0 0 1 2
1 3 4 5
2 6 7 8
31 93 94 95
32-bit transfer number (TN) 0~5
New row address (A_n)
0 ... 5
0 0
1 1
2 2
95 95
204

FIG. 3

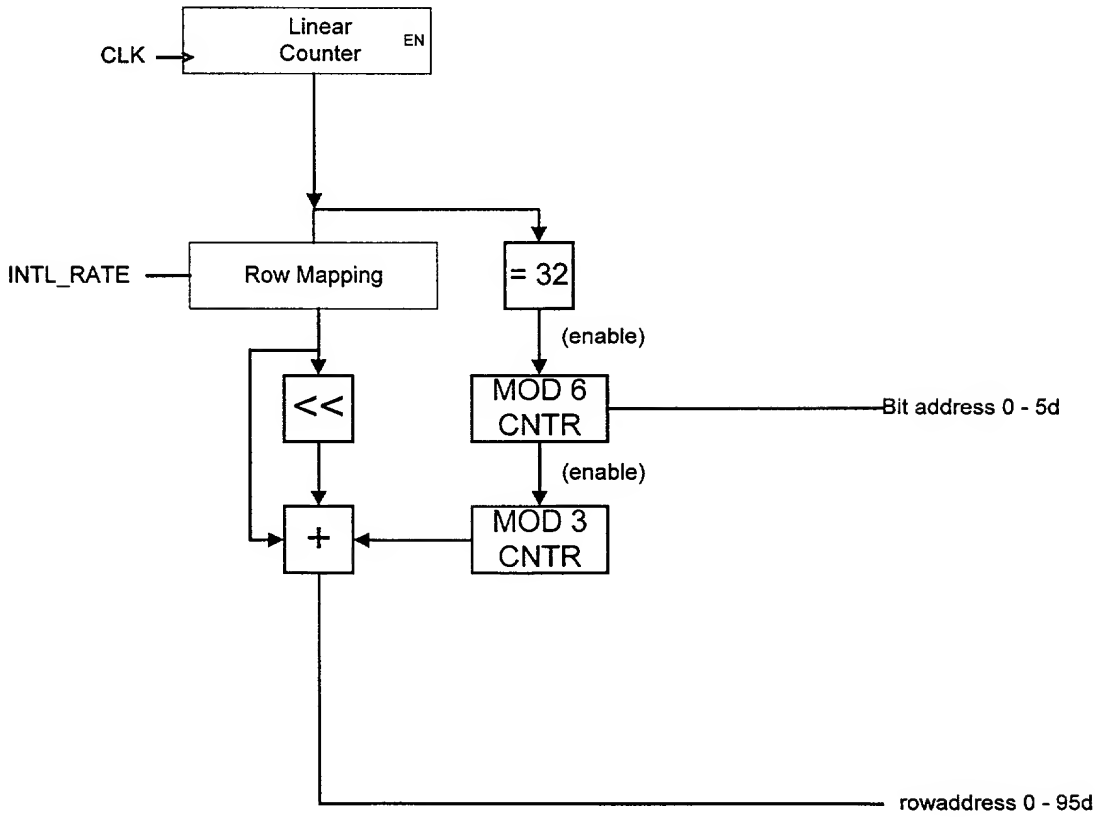

CLK
Linear Counter
EN
INTL_RATE
Row Mapping
= 32
(enable)
<<
MOD 6 CNTR
Bit address 0 - 5d
(enable)
+
MOD 3 CNTR
rowaddress 0 - 95d

FIG. 4

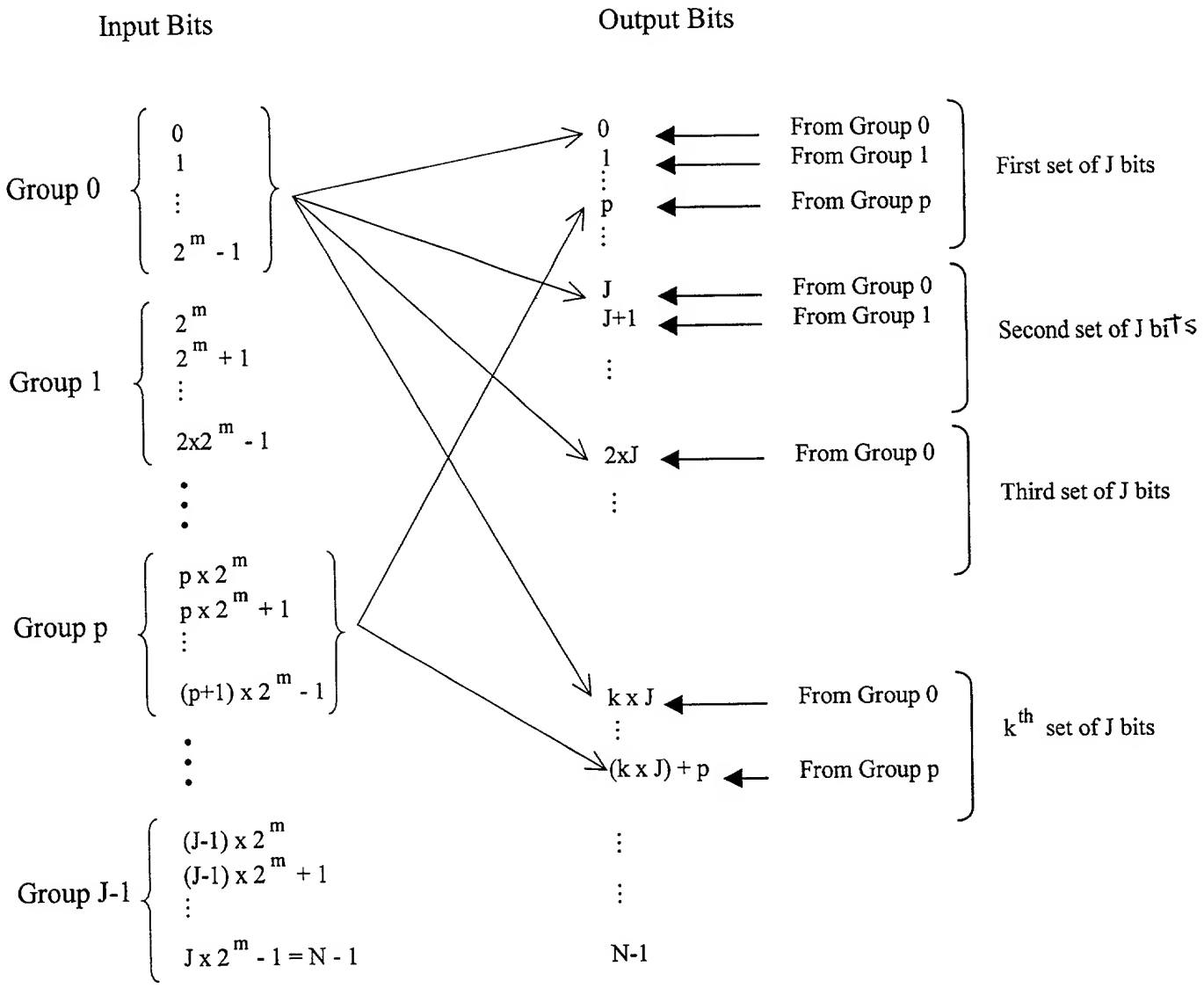

Input Bits
Output Bits
Group 0
0
1
2^m - 1
Group 1
2^m
2^m + 1
2x2^m - 1
Group p
p x 2^m
p x 2^m + 1
(p+1) x 2^m - 1
Group J-1
(J-1) x 2^m
(J-1) x 2^m + 1
J x 2^m - 1 = N - 1
0
1
p
J
J+1
2xJ
k x J
(k x J) + p
N-1
From Group 0
From Group 1
From Group p
From Group 0
From Group 1
From Group 0
From Group 0
From Group p
First set of J bits
Second set of J bits
Third set of J bits
k^th set of J bits

FIG 5

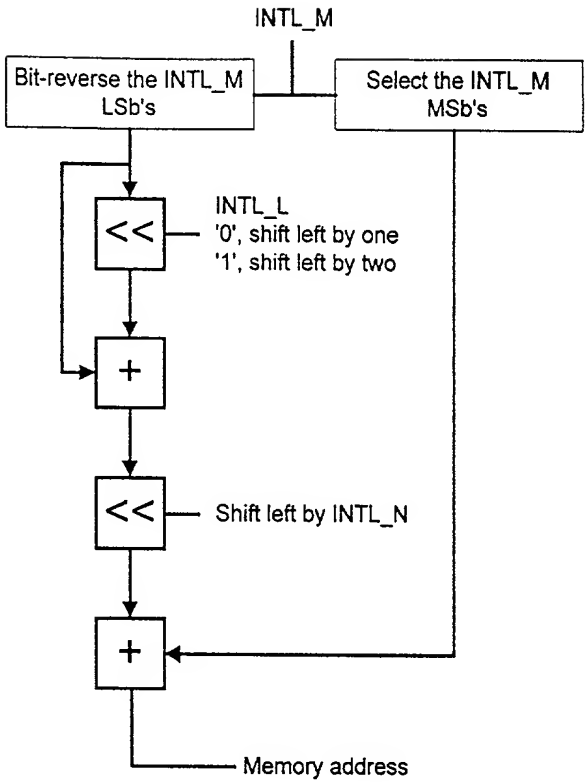
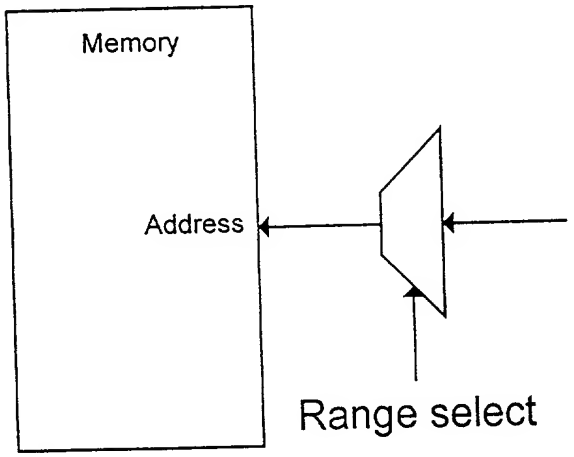


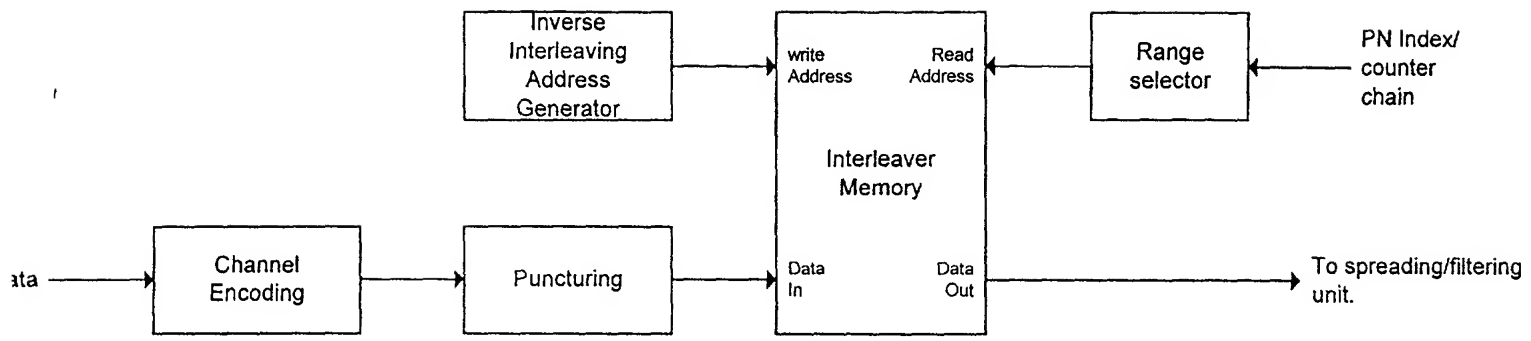
FIG. 6

Address[n:0] = Counter[(n+2):2]



PN Index or simple counter chain tied to reverse link frame timing.

FIG. 7


Inverse
Interleaving
Address
Generator
write
Address
Read
Address
Range
selector
PN Index/
counter
chain
Interleaver
Memory
ata
Channel
Encoding
Puncturing
Data
In
Data
Out
To spreading/filtering
unit.